EE 432 Advanced Digital Design with HDL
Spring 2013
Week 1

Lecture Topic and Reading Assignment for today
Reading - *EE432Overview-Spr2013*, *EE432ProjectOverviewSpr2013*, and browse the "Project Information" folder's files.

The lecture will cover the course, course project, and the operation of a PDP-8. I expect we will cover more details next week, and questions as the arise.

Homework Assignment #1, Due April 9 (next week)
Let's start out with just a few VHDL exercises. Implement the following modules in VHDL. Turn in a ZIP archive containing the VHDL source files for each problem. All synchronous circuits change state on the rising edge of the clock signal. You should verify that they work before turning them in.

1. A multiplexer has four data inputs *a1, a2, a3, a4* and a single output *y*. There are three control inputs, s1, s2, and s3. The output y should be a1 when s1=1, a2 when s2=1, a3 when s3=1, and s4 otherwise. It will never be the case that more than one control input is 1. All inputs and outputs are of type std_logic. Implement using a concurrent statement. (Hint — *when*)
2. Repeat problem 1, but this time use a process and no concurrent statements. (Hint — *if*)
3. Implement a synchronous counter with only *reset* and *clock* inputs, and outputs for the count equal 4 (named *cnt4),* 17, (named *cnt17),* 200, (named *cnt200)*, and 0 (named *cnt0*). The counter should reset to zero on the rising edge of the clock when either the *reset* input is 1 or the current count is 210. Note that the count is not an output port of the module.
4. Implement an 8-bit synchronous counter with *clock*, *load*, *up_enable*, and *down_enable* std_logic inputs, and a std_logic_vector(7 downto 0) input, *pload*. The counter has an std_logic_vector (7 downto 0) output named *count*. The counter is to load with the value *pload* if *load=1*, else it is to increment by one if *up_enable* = 1, else it is to decrement by one if *down_enable*=1. If none of load, up_enable, or down_enable is 1, the the counter is not to change.

Current Project Assignment
Study what you need to do to implement your part of the PDP-8. Meet with teammates before/after class, online, and/or at other times you can arrange. Be prepared to ask questions next week!

Don't forget to turn in your weekly Journal. The journal can be either a report of the last week or a running document that you add to continuously through the course. Add dates of any meetings.