EE 331 Digital Systems with HDL
Oregon Tech, Wilsonville, Winter 2014

Lab Assignment 7, due Week 9, March 4

In this lab you are to display the prime numbers stored in a ROM. The .coe file that defines the ROM contents has been provided in the distribution, primes.coe. The organization is 65536 words with 1 bit per word. The address represents the number being tested and the contents is 1 for prime and 0 for non-prime.

Your best approach will be to use lab assignment 5 solution as your starting point. The state machine needs to be modified so that each time the button is pressed (or held down so that a repeat occurs) the seven segment display should advance to the next prime. The state machine will require additional states to accomplish this. Additionally, the first prime (2) needs to be displayed when the program starts, not 0.

You will find that there is a problem in that the 7-segment display is 4 digits yet five digits are needed to display the primes. Display the most significant digit in binary using 3 LEDs in the row of LEDs.

The BCD counter cannot be used to address the ROM. You could create a circuit to convert BCD to binary, but will find it far simpler to have a 16-bit binary counter to drive the ROM address lines. Whenever you increment the BCD counter, increment the binary counter at the same time.

To turn in:

1. Report discussing what you did
2. VHDL source (with comments) for all modules incorporated in the document.
3. Design Summary showing successful synthesis.