EE 331 Digital Systems with HDL
Oregon Tech, Wilsonville, Winter 2014

Lab Assignment 6, due Week 8, February 25

Modify your lab assignment 5 design, adding two new buttons. One new button is to cause the counter to count by ten each time the button is pressed. This button should also repeat if held down, just like the first button. The second new button is to reset the counter to zero.

To accomplish this task you will first either need to replicate the button conditioning (synchronizer/filter/one-shot) circuitry by having three copies, or switch the signal path to use std_logic_vector(2 downto 0) for the three signals instead of std_logic. This latter approach will be cleaner and should be easier to implement.

The BCD counter will need two additional inputs for count by ten and reset, and you will have to made a couple of changes within the counter. While you are at it, change the digit counter to a procedure like we discussed in class.

You will need to modify the state machine, possibly adding new states, to handle the additional inputs and outputs.

To turn in:
1. Report discussing what you did
2. VHDL source (with comments) for all modules incorporated in the document.
3. Design Summary showing successful synthesis.